

II. CLAIMS

This listing of claims is provided as a courtesy to the Office, there are no changes.

1. (Previously presented) A semiconductor comprising:

a contact having a portion that extends on two opposing vertical sides of a vertical structure adjacent a first gate electrode, and wherein the contact contacts a diffusion adjacent the first gate electrode and is insulated horizontally from an adjacent second gate electrode and a spacer adjacent the second gate electrode by an insulating layer; and
a masking layer for insulating the first gate electrode from the contact.

Claims 2-3 (Cancelled).

4. (Previously presented) The semiconductor of claim 1, wherein the contact includes an upper portion that is larger than a lower contact portion.

Claims 5-20 (Cancelled).

21. (Previously presented) The semiconductor of claim 1, wherein the vertical structure is a spacer.

22. (Previously presented) The semiconductor of claim 21, wherein the contact contacts a substrate adjacent the spacer.

Claims 23-33 (Cancelled).

34. (Previously presented) A semiconductor comprising:

- a gate electrode;
- a spacer adjacent the gate electrode;
- a contact having a portion that extends on two opposing vertical sides of a first portion of the spacer, wherein the contact contacts a diffusion adjacent the gate electrode;
- an insulating layer having a portion that extends on two opposing vertical sides of a second portion of the spacer and contacts the gate electrode; and
- a masking layer contacting the gate electrode for insulating the gate electrode from the contact.

35. (Previously added) The semiconductor of claim 34, wherein the masking layer caps at least a portion of the gate electrode.

36. (Previously added) The semiconductor of claim 34, wherein the contact has an upper portion that is larger than a lower portion that contacts the diffusion.

Claims 37-42 (Cancelled).

43. (Previously added) The semiconductor of claim 35, wherein any remaining portion of the gate electrode is capped by the insulating layer.

44. (Previously presented) The semiconductor of claim 1, wherein the contact does not horizontally overlap the adjacent second gate electrode.

45. (Previously added) The semiconductor of claim 34, wherein the contact does not horizontally overlap an adjacent second gate electrode.